

Double Gated a-InGaZnO TFT Properties Based on Quantitative Defect Analysis and Computational Modeling

Hyunmin Hong^{ID}, Dong-Joon Yi^{ID}, Yeon-Keon Moon, Kyoung-Seok Son, Jun Hyung Lim^{ID}, KwangSik Jeong, and Kwun-Bum Chung^{ID}

Abstract—The device characteristics of amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistors (TFTs) were investigated using both single-gate (SG) and double-gate (DG) structures. The DG a-IGZO TFT demonstrated improved subthreshold swing (SS) and mobility compared to the SG structure. Moreover, in both positive and negative bias stresses (NBSs), the threshold voltage variation in the DG structure was significantly reduced. Quantitative analysis of activation energy and defect density indicated an increase in shallow-level defects and a decrease in deep-level defects within the DG structure. Additionally, based on quantitative defect measurements, the density of state (DOS) in a-IGZO was adjusted according to the structure, and the device properties and electric field distribution were simulated through TCAD. In the DG structure, the electric field was concentrated at both gates, resulting in an increase in bulk electric field intensity. Due to the increase in electric field, the average electron density within the channel in the DG structure increased by a factor of seven compared to the SG structure. This increase in electron density contributed to the enhancement of SS, mobility, and drive current. Additionally, there was a reduction in electron drift in the vertical direction within the channel, leading to an improvement in the stability of the device.

Index Terms—Computational modeling, defect analysis, double gate (DG) thin-film transistor (TFT), quantitative measurement.

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Hyunmin Hong, Dong-Joon Yi, KwangSik Jeong, and Kwun-Bum Chung are with the Department of Physics and Semiconductor, Dongguk University, Seoul 100-715, South Korea (e-mail: hmhong@dongguk.edu; iver.ydj@gmail.com; cks0701@dgu.ac.kr; kbchung@dongguk.edu).

Yeon-Keon Moon, Kyoung-Seok Son, and Jun Hyung Lim are with the Department of Display Research and Development Center, Samsung Display, Yongin 17113, South Korea (e-mail: ykeon.moon@samsung.com; kyoungseok.son@samsung.com; lanosjh.lim@samsung.com).

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I. INTRODUCTION

AMORPHOUS oxide semiconductors (AOSs) as the active layer in thin-film transistors (TFTs) have been studied extensively with a view to their application in various electronic devices, including in liquid crystal displays (LCDs) and active-matrix organic light emitting diodes (AMOLEDs). They offer superior electrical properties, a low-temperature fabrication process, and high optical transparency, compared to the conventional silicon-based TFTs. Among the numerous AOS materials, amorphous indium–gallium–zinc oxide (a-IGZO) is one of the most promising materials for use as the AOS TFTs channel, due to its high field-effect mobility (μ_{FE}) and uniformity over a large area. Nevertheless, as displays became high-resolution, higher mobility was required [1], [2], [3].

Recently, the double gate (DG) a-IGZO TFT has attracted attention for its remarkable advantages, such as excellent low turn-on voltage (V_{ON}) control and improved turn-on current, as two channels are formed by the voltage applied simultaneously to the upper and lower gate electrodes. Therefore, various electric circuits can be made by adjusting the positions and areas of the upper and lower channel layers to which the bias is applied. This results in a significant improvement in drain current due to the formation of parallel channel layers, compared to single channel layers in the single gate (SG) a-IGZO TFT devices. Moreover, by modulating the carrier transport path as well as the channel layer position and area, the interface carrier capture influence in DG TFT and the carrier surface scattering effect at the insulator–channel layer interface can be dramatically reduced. As a result, the carrier mobility and subthreshold swing (SS) can be improved [4], [5].

To apply the DG a-IGZO TFT to flat panel displays, it is essential to evaluate their electrical stability because long-term reliability must be guaranteed. The a-IGZO TFT instabilities under positive bias stress (PBS) have been explained by trapping in the gate dielectric, trapping in the bulk, or acceptor-like states creation [6], [7]. The last mechanism is supported by the parallel positive shift of the transfer curve observed during the PBS. On the other hand, the bulk donor state creation is the basis of a quantities model recently proposed to explain negative bias stress (NBS) [8], [9]. Therefore,

to analyze the instability of the device, it is necessary to analyze the defect state in detail.

Among methods for quantitatively analyzing defects, the photo-induced current transient spectroscopy (PICTS) method measures a transition current that changes over time by light and temperature. When light with energy higher than the bandgap is applied to the channel, electrons are trapped or de-trapped in the defect state. The activation energy and defect density can be analyzed by measuring the transition current as a function of temperature [10]. The PICTS can measure channel defects in an operating TFT by applying bias to the source/drain and gate. Therefore, it can analyze the dynamics of defects in the channel.

Semiconductor device design and simulation have become central elements in modern electronic technology. Simulation of semiconductor devices using TCAD involves numerically solving the fundamental semiconductor equations to calculate device characteristics. These basic semiconductor equations include device models that reflect the material properties and structure of each device. Therefore, an appropriate device model is necessary to describe the characteristics of a specific device. The device models used in the simulation include the density of states (DOSs) and carrier density-dependent mobility models. By adjusting the model parameters, various results can be obtained by comparing device characteristics with modeling outcomes [11].

However, these simulation models often rely on theoretical assumptions rather than being based on experimentally obtained data. Constructing a model with parameters that are not directly measured may result in a good fit to specific experimental data, but predictions under different conditions may be inaccurate. Furthermore, predicting the behavior of the model under new conditions or environments can be challenging, leading to questions about the predictive ability and physical reliability of the model. In contrast, an approach based on defect-based modeling, which directly measures and incorporates defects, is expected to provide higher accuracy and reliability compared to traditional theoretical modeling. This methodology is anticipated to lead to a better understanding of the operating mechanism of the device and improve the prediction of its behavior in real-world environments.

In this study, we utilize experimentally obtained activation energy and defect density to simulate the electrical characteristics of an SG and DG TFT using TCAD. Furthermore, the instability results are compared with those of SG TFTs. Based on the results of quantitative defect analysis, the electron density distribution of the channel is simulated to improve accuracy, and the origin of enhancement in stability of the DG device can be understood based on the improved simulation.

II. EXPERIMENTS

A. Device Fabrication

Fig. 1(a) and (b) show schematic cross sections of the SG and DG a-IGZO TFTs. A Mo layer was deposited on glass and patterned as the bottom metal layer (BML) electrode, and a 200 nm thick SiO_x layer was then deposited as the buffer layer. The Mo and GI layers were patterned continuously by

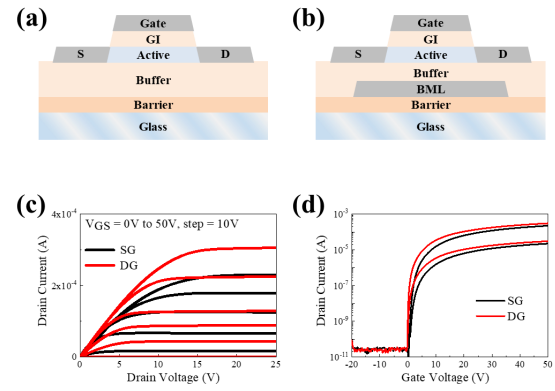


Fig. 1. Cross-sectional schematic. (a) SG. (b) DG a-IGZO TFT. (c) Output characteristics and (d) transfer characteristics at $V_D = 0.1$ and 20 V.

photolithography. The BML acts as a bottom gate, and when measuring the device, the same bias as the gate electrode is applied to the BML, resulting in a DG device. An active layer of 30 nm thick a-IGZO was formed by sputtering. On the active layer, a 140 nm thick SiO_x was deposited as the gate insulator. Then, Mo was sputtered as the top gate-source, and drain electrodes. The fabricated TFTs had a channel width (W) and length (L) of (3 and 5) μm , respectively.

B. Physical Analysis

To quantitatively analyze the defect state using PICTS, the a-IGZO TFT was irradiated with an LED ($\lambda = 405$ nm) and the photocurrent was measured in the range (280–320) K.

The device characteristics of the a-IGZO TFTs were measured using a semiconductor parameter analyzer. Drain current (I_D) was measured under a gate voltage (V_{TG} , V_{BML}) sweep from (–10 to 30) V and by maintaining a constant drain voltage (V_D) of 0.1 and 20 V.

III. RESULTS AND DISCUSSION

A. Device Characteristics

Fig. 1(c) and (d) show output and transfer characteristics for each structure. It can be observed that the current in the DG structure is significantly higher than that in the SG structure. This shows that the current in the DG structure is improved more efficiently compared to the SG structure. The threshold voltage (V_{th}) was defined as the value of gate voltage (V_G) inducing the I_D of 10 nA. The situation mobility (μ_{sat}) of the a-IGZO TFT device was obtained from the drain current in the linear region by using the following equation:

$$\mu_{sat} = \frac{L}{\frac{1}{2}C_{ox}W} \left(\frac{d\sqrt{I_D}}{dV_G} \right)^2 \quad (1)$$

where C_{ox} is the gate insulator capacitance per unit area. The threshold voltages in the initial sweep of SG structure and DG structure are (1.87 and 1.54) V at $V_D = 0.1$ V and (0.86 and 0.59) V at $V_D = 20$ V. The saturation mobility of the SG structure and DG structure is (16.83 and 27.36) $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ at $V_D = 0.1$ V and (22.37 and 34.77) $\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ at $V_D = 20$ V. The SS of the SG and DG structure is

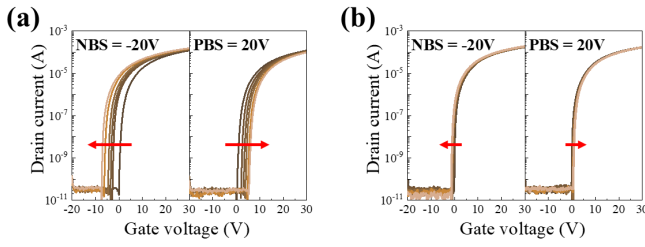


Fig. 2. Device instability of the a-IGZO-TFTs by gate bias stress. (a) SG. (b) DG.

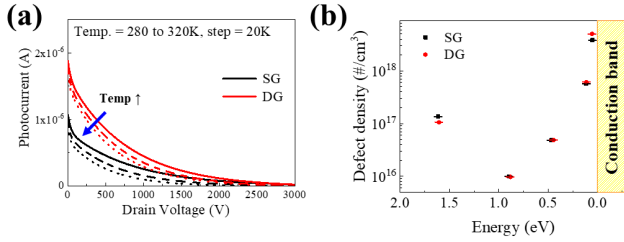


Fig. 3. (a) Decay of photocurrent with temperature. (b) Quantitative defect measurement results using PICTS according to structure.

(0.62 and 0.30) $\text{V}\cdot\text{decade}^{-1}$ at $V_D = 0.1$ V and (0.39 and 0.28) $\text{V}\cdot\text{decade}^{-1}$ at $V_D = 20$ V. The device characteristics are better at $V_D = 20$ V [12]. Regardless of V_D , in the DG structure, the threshold voltage is similar, but the mobility and SS The value has been greatly improved.

To evaluate the long-term reliability of the device, a gate bias of ± 20 V was applied for a total time of 5,400 s. Fig. 2(a) and (b) show the transfer curve shift (ΔV_{th}) according to the SG and DG structures. In the SG structure, ΔV_{th} according to NBS and PBS shifted by (-7.60 and 5.03) V, while in the DG structure, they shifted by only (-1.03 and 0.76) V, respectively. There was no significant change in the SS value. Device performance, such as the SS value, mobility, and bias instability (ΔV_{th}), is affected by defects at the channel/dielectric interface [13]. Therefore, a detailed analysis of the distribution and types of defects is required to understand device characteristics that are significant reductions in ΔV_{th} by electrical stress.

B. Quantitative Defect Analysis

Fig. 3(a) shows the decay of photocurrent according to the structure. At 0 s, the photocurrent in the DG structure is observed to be higher compared to the SG structure. As the temperature increases, the photocurrent in each structure decays more rapidly. For PICTS analysis, the photocurrent is subjected to Laplace inversion transform to extract the decay constant, and the decay behavior is examined as a function of temperature [14]. Fig. 3(c) and Table I show the result of quantitative analysis for the defect energy and density according to the TFT of SG and DG structure. Defect states in the bandgap act as electron trapping and scattering sites, and depending on their energy and density, can have different effects on the TFTs [15]. According to the Fermi-Dirac statistics, the activation energy that can be transferred to the conduction band at room temperature (RT) is less

TABLE I
ACTIVATION ENERGY (E_a) AND DEFECT DENSITY (N_0) BY PICTS ACCORDING TO STRUCTURE

Single gate		Double gate	
E_a (eV)	N_0 (cm^{-3})	E_a (eV)	N_0 (cm^{-3})
0.052 ± 0.011	$382 \pm 5.12 \times 10^{16}$	0.053 ± 0.005	$503 \pm 8.39 \times 10^{16}$
0.113 ± 0.008	$56.6 \pm 1.13 \times 10^{16}$	0.113 ± 0.007	$60.7 \pm 1.21 \times 10^{16}$
0.468 ± 0.015	$485 \pm 9.54 \times 10^{14}$	0.445 ± 0.013	$486 \pm 9.76 \times 10^{14}$
0.896 ± 0.032	$99.9 \pm 2.07 \times 10^{14}$	0.882 ± 0.027	$97.9 \pm 1.54 \times 10^{14}$
1.615 ± 0.016	$136 \pm 2.71 \times 10^{15}$	1.606 ± 0.024	$105 \pm 2.38 \times 10^{15}$

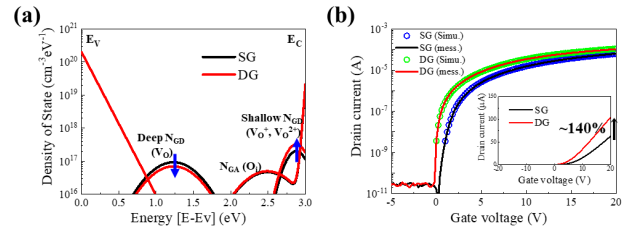


Fig. 4. (a) DOS of a-IGZO TFT for TCAD simulation based on quantitative defect measurements and (b) measured (line) and TCAD-simulated (circle) transfer curves.

TABLE II
MODEL PARAMETERS USED FOR A-IGZO MATERIAL

	SG	DG
N_{GA} ($\text{cm}^{-3}\text{eV}^{-1}$)	3.50×10^{16}	3.78×10^{16}
N_{GD} ($\text{cm}^{-3}\text{eV}^{-1}$)	1.99×10^{17}	2.81×10^{17}
N_{TA} ($\text{cm}^{-3}\text{eV}^{-1}$)	3.72×10^{19}	4.03×10^{19}
W_{TD}		0.2
N_{TD} ($\text{cm}^{-3}\text{eV}^{-1}$)	1.85×10^{20}	1.52×10^{20}
W_{TA}		0.015

than 0.25 eV, defects that exist at that energy are said to be shallow defects, and electrons trapped in these defects can be easily dissociated at RT, and act as carriers by the hopping process [16]. Defect levels larger than 0.25 eV are deep-level defects and electrons trapped in those defects can be released during device operation, increasing charge carrier scattering and reducing their mobility [17]. When comparing the defects of the SG and DG structures, there is no significant difference between the defect energies of the two structures. The shallow level defect densities are $(4.39$ and $5.63) \times 10^{18} \text{ cm}^{-3}$, while the deep level defects are $(1.94$ and $1.64) \times 10^{17} \text{ cm}^{-3}$. Within the measurement error range, there was a clear distinction in defect density between the two structures. The DG structure has greater shallow-level defect density and lesser deep-level defect density. Therefore, the DG structure increases carrier concentration and reduces electron scattering, thereby improving device stability.

C. Computational Modeling

Fig. 4(a) and Table II show the DOS utilized to model the measured data for TFTs in SG and DG structures.

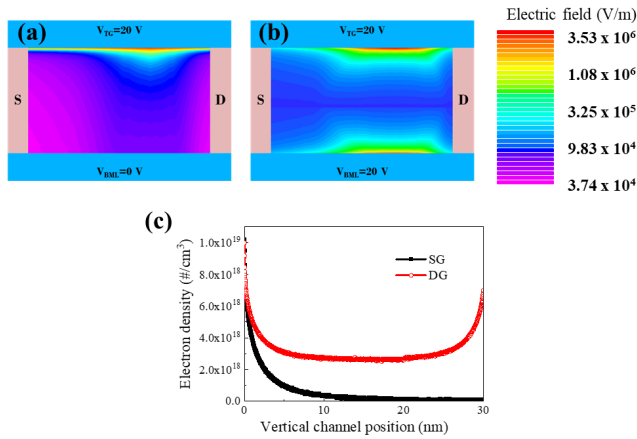


Fig. 5. TCAD-simulated electric field distribution. (a) SG. (b) DG. (c) Simulated electron density at vertical channel positions.

In contrast to previous paper used the same DOS model to simulate TCAD for SG and DG structures, our simulations adjusted DOS of DG structure based on quantitative defect measurement results [18]. In the a-IGZO material, sub-gap states are predominantly categorized as acceptor-like and donor-like states, represented by Gaussian distribution states and exponentially decaying band-tail states [19]. The Gaussian curve incorporates two donors (N_{GD}) and one acceptor (N_{GA}) corresponding to deep donor states ($N_{GD}(V_o)$), oxygen interstitials ($N_{GA}(O_i)$), and shallow donor states ($N_{GD}(V_o^+/V_o^{2+})$), respectively. Compared to the SG structure, the DG structure augments the carrier concentration due to an increase in shallow donor states, while electron scattering diminishes owing to a decrease in deep donor states. In Fig. 4(b), the solid line represents the experimental data, and the circles represent TCAD fitting with different DOS, demonstrating good agreement between experimental data and simulation results. Consequently, the drive current of the DG structure exhibits a 140% increase at a 20 V overdrive compared to the drive current of the SG structure [inset Fig. 4(b)].

Since the channel deposition conditions are the same, differences in DOS depending on the structure occur depending on the structure. To observe various electronic properties (electric field, electron concentration) depending on the structure, simulations were performed using horizontal cutting lines in ATLAS TCAD. The gate and S/D overlap of $1 \mu\text{m}$ is used. Fig. 5(a) and (b) show the electric field for the SG structure with $V_{TG} = 20$ V and DG structure with $V_{TG} = V_{BML} = 20$ V, respectively. The electric field attracts or repulses electrons according to the polarity of the applied gate bias and drifts more electrons according to electric field intensity. In the SG structure, the electric field is strongly concentrated only on the top gate. On the other hand, the electric field in the DG structure is concentrated on both the top gate and the BML. The bias applied to both gates causes a partial cancellation of the electric field near each gate, leading to a slight decrease. However, the electric field in the central region of the channel increases. As a result, the electric field difference between the center of the channel and the edge of gate is decreased, and the electric field becomes more uniformly distributed throughout

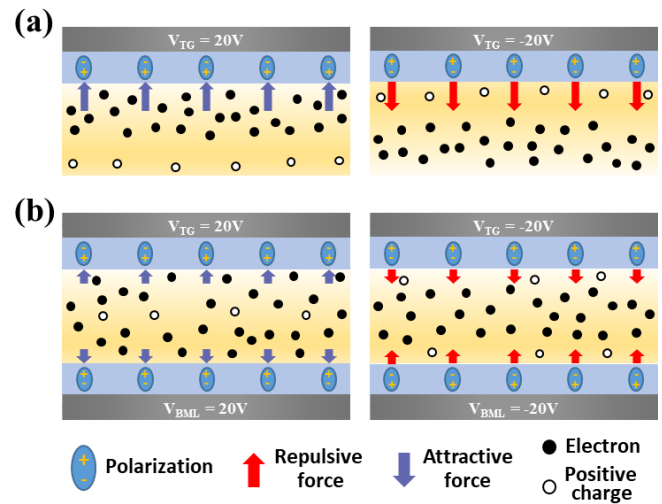


Fig. 6. (a) Schematic of electron movement in the a-IGZO active layer when gate bias stress is applied. (a) SG. (b) DG.

the entire channel [20], [21]. Fig. 5(c) shows the electron densities for the vertical structure at the center of the channel in the SG and DG structures calculated via electric fields simulated with TCAD. In the channel, the top of the channel is 0 nm, while the bottom of the channel is 30 nm. In the SG structure, since gate bias is applied only to the top of the channel for TFT operation, electrons are concentrated only at the top, and electrons in the bulk are reduced. In the DG structure, since the gate bias is applied to both the top and bottom of the channel for TFT operation, electrons are highly distributed on both sides of the channel, and electrons in the bulk remain at a constant level. (Since 200 nm thick SiO_x , which is thicker than the top gate insulator, is placed on the BML, the electric field at the bottom of the channel is weak, and the electron density is low, compared to the top of the channel.) At 0 nm, the electron density is $1.02 \times 10^{19} \text{ cm}^{-3}$ in the SG structure and $9.78 \times 10^{18} \text{ cm}^{-3}$ in the DG structure, i.e., larger in the SG structure. However, the average electron density of the entire channel region is $4.07 \times 10^{17} \text{ cm}^{-3}$ in the SG structure and $2.96 \times 10^{18} \text{ cm}^{-3}$ in the DG structure, i.e., larger in the DG structure. Consequently, this increase in the electron accumulation area in the a-IGZO channel region is associated with a shallow donor state, leading to an increase in free electrons and drain current.

Fig. 6(a) and (b) show the electron movement of the active layer according to the structure of the a-IGZO TFT when the gate bias is applied. When a positive bias is applied to the gate of the a-IGZO TFT, electrons diffuse in the direction of the insulator, due to attractive force according to the polarity of the gate insulator. These electrons drift at the interface of the insulator, forming occupied states, and increasing the relative area of the conduction band. The occupied state increases when the PBS time is increased or when a larger gate bias is applied. On the other hand, when a negative bias is applied, electrons drift to the opposite side of the insulator, forming unoccupied states at the interface. This is related to an increase in free electrons provided in the weakly bonded unstable defect state. To understand the occupied/unoccupied state caused

by the gate bias in the DG structure, the interaction of the biases applied to both gates must be considered. In the DG structure, when a gate bias is applied to both ends, an area of constant electron density is formed in the center of the channel at (10~20) nm, which reduces the number of electrons drifting to both ends of the channel. Compared to the SG structure, the number of electrons drifting in the vertical direction decreases, reducing the probability of electrons being captured and scattered in the deep donor state [5]. As a result, the electric field in the center of the channel is maintained stably, which improves not only the SS and mobility of the device, but also stability.

IV. CONCLUSION

Defect analysis and device computational modeling are employed to understand the cause of the difference in device characteristics for the SG structure and the DG structure. Compared to SG, the DG structure demonstrates improved device characteristics, such as SS and saturation mobility. In addition, the instability of the DG structure under positive and NBS is also improved with reduction in ΔV_{th} to (−1.03 and 0.76) V. In the quantitative defect measurement, the DG structure shows a higher density of shallow level defect and a lower density of deep level defect than the SG structure. Based on quantitative defect analysis, the DOS of the DG structure was modified to increase shallow donors and decrease deep donors. In the DG structure, the carrier concentration increases and the scattering of electrons decreases, resulting in increased SS and saturation mobility. Additionally, simulations of the electric field distribution in the channel show that the DG structure has a larger space charge area than the SG structure. The electric field in the center of the channel remains stable, improving device stability. Unlike previous papers, the results of this study show that DOS can be adjusted depending on the structure, and are expected to be helpful in simulating and analyzing device characteristics through quantitative defect measurements.

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